REMARKS

The present invention is directed to a multilayer printed circuit board comprising a resin substrate board having, on both sides thereof, first resin insulating layers each comprised of the same resin material; and a lower metal layer, having a conductor circuit having the same pattern as said lower metal layer, on each of said first resin insulating layers.

In the Office Action mailed December 28, 2005, claims 25, 26, 29, 64 and 65 were rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over JP 3-229484 to Kaizu Masahiro ("JP '484") in view of Wroe et al (U.S. Patent 4,994,903). Further, claims 30-32, 67 and 68 were rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over JP '484 in view of Wroe et al and further in view of Brandi et al (U.S. Patent 5,227,012).

In the present Amendment, claims 25, 26 and 30 have been amended to improve their form, which does not narrow the scope of the claims. Claims 69 and 70 have been added. Claim 69 is supported, for example, by lines 2 to 3 on page 58, lines 8 to 9 on page 32, and lines 10 to 17 on page 151 of the specification. Claim 70 is supported, for example, by Fig. 25(d) of the specification. Claims 1-24, 27, 28, 33-63 and 66 were previously canceled. No new matter has been added and entry of the Amendment is respectfully submitted to be proper. Upon entry of the Amendment, claims 25, 26, 29 - 32, 64, 65 and 67-70 will be all the claims pending in the application.

I. Forms PTO/SB/08 A & B

The Examiner is respectfully requested to initial and date the Forms PTO/SB/08 A & B filed with Applicants' Information Disclosure Statements of December 21, 2005 and January 10, 2006, and return a signed copy to Applicants' representatives in the next PTO communication.

II. Response to Rejections under 35 U.S.C. § 103(a)

In Paragraph No. 4, at page 3 of the Office Action, claims 25, 26, 29, 64 and 65 were rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over JP 3-229484 to Kaizu Masahiro ("JP '484") in view of Wroe et al (U.S. Patent 4,994,903). Further, in Paragraph No. 5, at page 5 of the Office Action, claims 30-32, 67 and 68 were rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over JP '484 in view of Wroe et al and further in view of Brandi et al (U.S. Patent 5,227,012).

Applicants respectfully submit that the present claims are patentable over the cited references for at least the following reasons.

a. The present invention

According to the present invention, the multilayer printed circuit board comprises a resin substrate board, a first resin insulating layers on both sides of the resin substrate board, and a lower metal layer on each of the first resin insulating layers. A conductor circuit is further constructed on the lower metal layer.

Since the lower metal layer has a high adhesion to the first resin insulating layer, the resin insulating layer can obtain a firm adhesion to the conductor circuit without providing a roughened layer on the surface thereof. As a result, the surface of the conductor circuit becomes flat so that no signal conduction delay occurs even when high-frequency signals are used (see page 54, line 30 to page 55, line 2 in the specification). The lower metal layers may contain at least one metal selected from the group consisting of Al, Fe, W, Mo, Sn, Ni, Co, Cr, Ti and noble metals (clam 26).

Further, according to the present invention, the resin insulating layer comprise thermosetting polyolefin resin. Polyolefin resin has high adhesion to conductor circuits so that the conductor circuits can be constructed without roughening the surface of the resin insulating layer. Thus, the conductor circuit can be formed directly on the smooth surface of the resin insulating layer (page 57, lines 14 to 18 in the specification).

Furthermore, the polyolefin resin has dielectric constant values and dielectric loss tangent values lower than the corresponding values of an epoxy resin. Therefore, compared with epoxy resin insulating layers, there is no signal conduction delay in the polyolefin resin insulating layers even when high-frequency signals are carried. Moreover, the polyolefin resin is comparable to an epoxy resin in terms of heat resistance so that no stripping of the conductor circuit occurs even at the solder melting temperature. In addition, because of the high fracture rigidity of the polyolefin resin, there is no risk of cracks originating from the interface between

the conductor circuit and the resin insulating layer under the conditions of the heat cycle test (see page 57, lines 19 to 30 of the specification).

b. JP '484

JP '484 discloses a method of manufacturing a printed wiring board. As shown in Figs. 2(A) to 2(D), the printed wiring board comprises the base insulating material layer 10, the adhesive layer 11 comprising an epoxy resin, the metal film 12 comprising nickel, the copper conductor circuit 14, and the metal film 13 comprising nickel covering the metal film 12 and the copper conductor circuit 14 (see Example). JP '484 teaches that the metal films 12 and 13 prevent migration, and also prevent peeling of the conductor circuit 14 (see page 5, upper left column). Metal such as Ni-Ag, Pd-Ni or Au, and a complex layer thereof can be used instead of nickel to prevent migration (see page 4, upper left column).

However, as the Examiner notes, JP '484 does not teach using a polyolefin resin as the adhesive layer 11.

As set forth above, an epoxy resin layer has dielectric constant values and dielectric loss tangent values higher than those of a polyolefin resin. The epoxy resin layer may cause signal conduction delay when high-frequency signals are carried. Further, fracture rigidity of an epoxy resin is lower than that of a polyolefin resin. Thus, it is likely that the epoxy resin layer has cracks originated from the interface between the conductor circuit and the resin layer under heat cycle test, and the nickel film 12 (and the copper conductor circuit 14) may be stripped off.

Since the surface of the epoxy adhesive layer 11 is flat (see Fig. 2), it is more likely that the nickel film 12 and the copper conductor circuit 14 are stripped off. Therefore, the effects of the present invention (e.g., prevention of cracks and stripping by the polyolefin resin) cannot be attained in JP '484.

c. Wroe et al

Wroe et al discloses a circuit substrate. The substrate 12 comprises the electrically insulating layer 24 of an organic electrically insulating material having a multiplicity of dispersed particles 28. The organic material of the electronically insulating layer 24 is, for example, epoxies or polyolefins (col. 3, lines 8 to 25). On one side 24.1 of the substrate 12, the semiconductor device 18, the circuit paths 14 and the like are arranged. The substrate 12 further comprises, on the other side of the electrically insulating layer 24, the heat-sink layer 30 comprising the first metal layer 30.1 and the second metal layer 30.5 (which correspond to the layers 30.6 to 30.8). The second layer 30.5 comprises, for example, copper or aluminum (col. 3, lines 40 to 53).

Wroe et al does not teach forming another metal layer on the heat-sink layer 30. Namely, Wroe et al does not teach a metal layer corresponding to the conductor circuit of the present invention. Further, the heat-sink layer 30 is formed to dissipate heat generated in the circuit (col. 4, lines 46 to 48), rather than to ensure a firm adhesion between the electrically insulating layer and another metal layer. The heat-sink layer 30 of Wroe et al does not meet the requirements of

the lower metal layer in the present invention. Furthermore, the effects of the present invention (e.g., a firm adhesion ensured by the lower metal layer) cannot be attained in Wroe et al.

Although Wroe et al teaches that polyolefins can be used to form the electrically insulating layer 24, it does not teach that polyolefins have a good adhesion to a metal layer. Accordingly, one of ordinary skill in the art would not have been motivated to substitute the polyolefin resin layer described in Wroe et al for the epoxy resin layer, as the adhesive layer 11, in JP '484. Moreover, there is no reasonable expectation that the polyolefin resin layer described in Wroe et al would provide sufficient adhesion to the metal layer in JP '484.

In addition, Brandi et al does not make up for the deficiencies of JP '484 in view of Wroe et al.

In view of the foregoing reasons, Applicants respectfully submit that the present claims are not obvious over the cited references.

Further, none of the cited references teach or suggest the dielectric constant value and the dielectric loss tangent value of the material of the insulating layer. For this reason additionally, Applicants respectfully traverse the rejection of claim 65.

Accordingly, the Examiner is respectfully requested to reconsider and withdraw the rejections.

III. New Claims 69 and 70

Claim 69 requires that the resin substrate board is a copper-clad laminate. The copper-clad laminate has a higher rigidity compared to the base insulating material layer 10 of JP '484, which is made of a polyimide film. Using a copper-clad laminate, warpage of the substrate board and peeling of the conductor circuit can be prevented. Further, since the buildup structure is formed on each side of the resin substrate board in the present invention, fine patterns can be provided. Therefore, claim 69 is novel and patentable over the cited references.

Claim 70 requires that the upper metal layer is formed on the whole surface of said conductor circuit. Since the upper metal layer is composed of at least one metal selected from the group consisting of metals (exclusive of Cu) of the 4^{th} through 7^{th} periods in Group 4A through Group 1B of the long-form periodic table of the elements, Al, and Sn, it has a high adhesion to the resin insulating layer or the solder resist layer. Thus, the entire surface of the conductor circuit can obtain a firm adhesion to the resin insulating layer or the solder resist layer formed on the upper metal layer. Therefore, claim 70 is novel and patentable over the cited references.

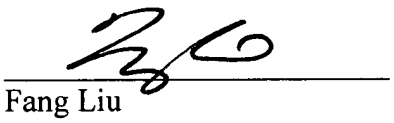
IV. Conclusion

In view of the above, reconsideration and allowance of claims 25, 26, 29, 32, 64, 65 and 67-70 are now believed to be in order, and such actions are hereby earnestly solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or

telephone interview, the Examiner is kindly requested to contact the undersigned at the local D.C. telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



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